

FIG. 1

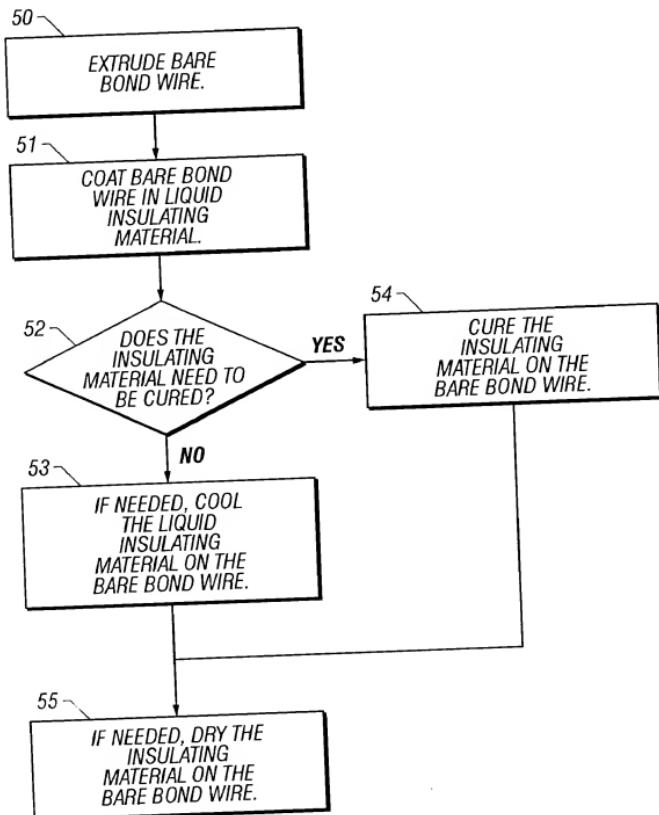


FIG. 2

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INSULATED BOND WIRE ASSEMBLY PROCESS TECHNOLOGY  
FOR INTEGRATED CIRCUITS  
Harry Q. Pon

3/5

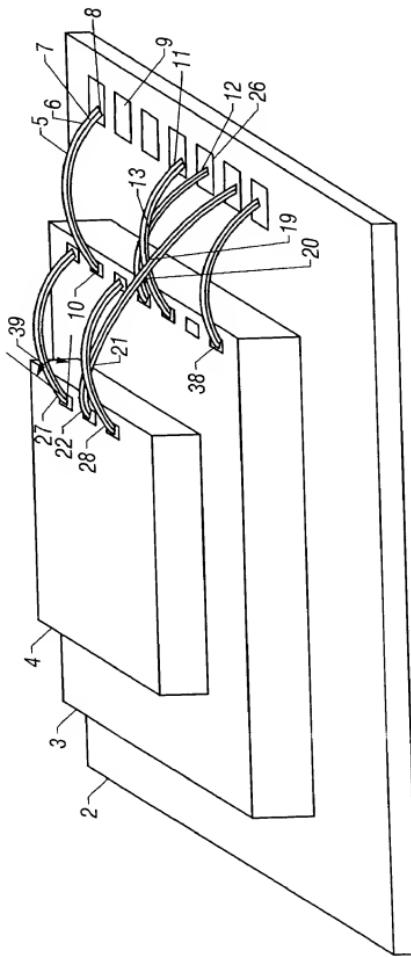


FIG. 3

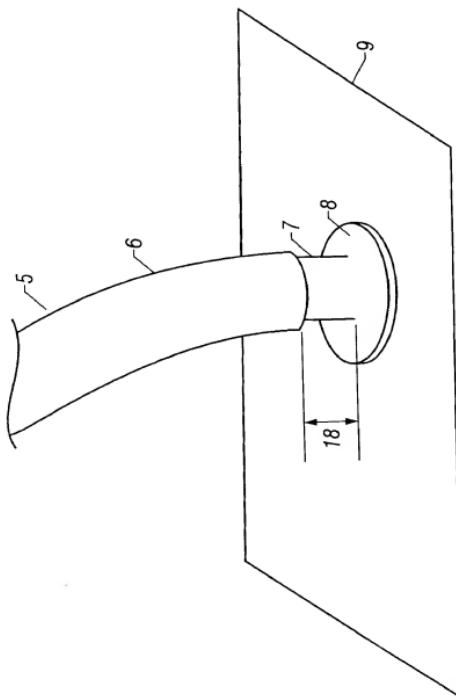


FIG. 4

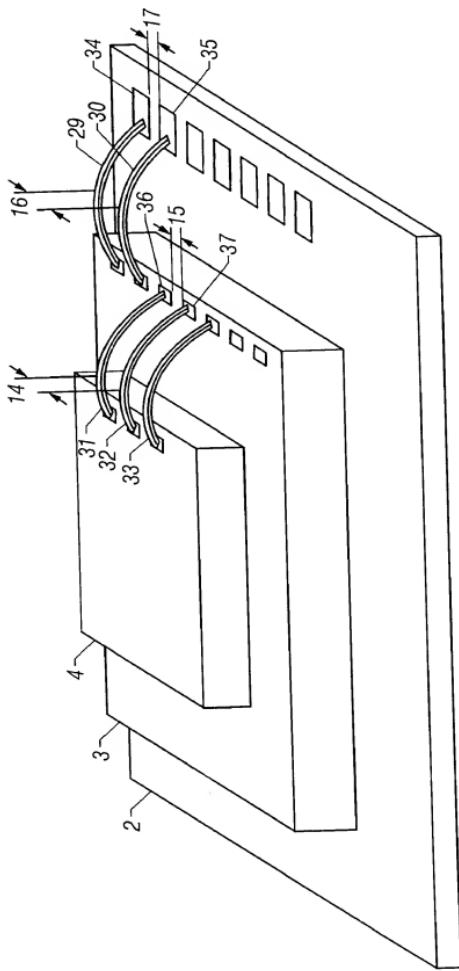


FIG. 5